an etching-stop layer formed on said main surface of said substrate; and

an insulation layer formed on said etching-stop layer,

said semiconductor device further comprises a single damascene structure via hole provided on a main surface of said insulation layer and penetrating through said insulation layer and said etching-stop layer so that a bottom of said via hole reaches at a surface of said interconnect layer, and a barrier layer continuously covering said main surface of said insulation layer, an inside wall surface of said via hole and the surface of said interconnect layer integratedly.

In the Abstract

Please cancel the original Abstract.

A new Abstract related to a semiconductor device is attached herewith.

In the drawings

Subject to approval by the Examiner in charge, enclosed herewith are sketches of Figs. 1(a)-1(c) and 2(a)-2(c) with corrections shown in red.

REMARKS

In response to the outstanding Office Action. Applicant amended the specification and the drawings to correct inaccuracies.

Claim 1 is pending in the present application. Claims 2-11 are withdrawn from consideration.

Claim 1 has been herein amended to overcome the rejection under 35 U.S.C. §112, second paragraph and to more clearly distinguish over the art.

Claim 1 is rejected under 35 U.S.C. §102 as being anticipated by Zhao et al., (6,037,664).

The Examiner states that Zhao et al. discloses the claimed semiconductor device comprising a substrate 11, an interconnect layer 10 of copper formed along with a predetermined pattern in buried condition. a silicon nitride layer 13 formed on the main surface of the substrate, an insulation layer 14 on the silicon nitride layer and a via 24 penetrating through the insulation layer and silicon nitride layer so that a bottom of the via hole reaches at a surface of the interconnect layer and a barrier layer 28 continuously covering the main surface of the insulation layer, inside wall of the via hole and the surface of the interconnect layer 10 integratedly.

The Examiner's attention is respectfully directed to column 4, lines 15-25 and column 5, lines 45-52 of the reference. Contrary to the present invention as claimed, conductive region 10 of the reference resides within a dielectric layer 11 which is not a substrate. According to Zhao et al. a region which underlies the interconnect 10 can be a conductive, dielectric or semiconductor region which may be a substrate itself.

Zhao et al. discloses a complex multilayer structure comprising a dual damascene interconnect structure, whereas a three-layer structure including a substrate and a single damascene structure via hole forms a semiconductor device with a barrier film of the present invention.

The interconnect 10 of the reference is not buried in the substrate.

Furthermore, in Zhao, there are two etching-stop layers 15 and 19, which are not formed on a main surface of a substrate, contrary to claim 1, (see column 6, lines 23-28, 59-60; Fig. 6). Layer 13, alleged by the Examiner to be equivalent to the etching-stop layer in claim 1, (Office Action, paragraph 9, pages 3-4), is provided on layer 11 with the interconnect therein, (see column 6, lines 23-28), and layer 13 is a barrier layer on which

dielectric layer 14 is deposited, instead of an etching-stop layer.

Since claim 1 provides for a single damascene structure via hole, instead of the double damascene interconnect structure of Zhao et al., one of the two etching-stop layers, 15 and 19, disclosed in Zhao et al. would clearly be unnecessary in the invention as claimed in claim 1.

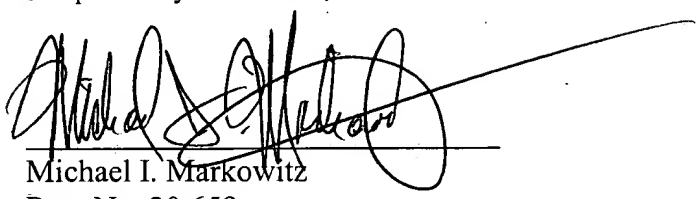
Accordingly, it is believed that claim 1 as amended is patentably distinguishable over the prior art and should be allowed.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached pages are captioned "Version with markings to show changes made."

In view of the above amendments and remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper, not fully covered by an enclosed check, may be charged to Deposit Account 50-1290.

Respectfully submitted,



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Enclosure: Version With Markings to Show Changes Made
Figs. 1(a)-1(c) and 2(a)-2(c)

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ABSTRACT OF THE DISCLOSURE

A semiconductor device has a substrate and a $5i0_2$ layer/etching-stop layer/Cu layer laminate, in which a via hole is formed, which is patterned. A barrier film is formed onto the via hole, which continuously covers the main surface of the $5i0_2$ layer, the inside wall surface of the via hole and a surface of the Cu layer integratedly.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the specification

The last paragraph at page 1 has been amended as follows:

This problem with the prior art method is illustrated in more detail in Fig. 2(a), Fig. 2(b), and Fig. 2(c). As shown in Fig. 2(a), a resist [layer/$5i0_2$ layer/Cu interconnect] layer 11, a Si0~ layer 12 and a Cu inter-connect layer 13 are formed at a first step, and a via hole 17 extending to the copper interconnect layer 13 is formed at the second step.

The paragraph at page 2, lines 2-8 has been amended as follows:

At this step, copper on the surface of the copper interconnect layer acts on the via hole side surface so as to form a copper deposition 14 on the side surface, this side surface copper deposition being a cause of leakage current.

In addition. there is oxidation 15 of the copper surface of the copper interconnect layer, this oxidation leading to an increase in electrical resistance. The barrier performance of [the] a TaN barrier film 16 formed as shown in Fig. 2(c) is weak in the barrier characteristic.

The paragraph at page 4, lines 9-19 has been amended as follows:

A first aspect of the present invention is a semiconductor device which comprises, a substrate, on a main surface of which, interconnect layers made at least of copper are formed along with a predetermined pattern in buried condition. an etching-stop layer formed on the main surface of the substrate, and an insulation layer formed on the etching-stop layer, and wherein the semiconductor device further comprises a via-hole provided on a main [surfacer] surface of the insulation layer and penetrating through the

insulation layer and the etching-stop layer so that a bottom of the via hole reaches at a surface of the interconnect layer, inside wall surface of the via hole and surface of the interconnect layer integratedly.

The paragraph at page 6, lines 5-16 has been amended as follows:

The basic method for producing the via hole 20 in a semiconductor device 30 of the present invention comprising, a step of forming a first step via hole (5) in a laminated structure formed by a copper layer (1), an etching-stop layer (2) on the surface side of the copper layer (1), and [a] an insulation layer (3) on the surface side of the etching-stop layer (2), a step whereby the formation of the first step via hole (5) is stopped by the etching-stop layer (2), and a second step via hole (6) is further formed so as to continue from the first step via hole (5), thereby forming [a] the via hole 20 a step whereby the second step via hole (6) extends to the copper layer (1) and the second step via hole (6) is cleaned, and a step, after the above-noted cleaning, whereby a barrier film (7) is formed on the first step via hole (5) and the second step via hole (6) by sputtering.

The paragraph at page 8, lines 2 1-24 has been amended as follows:

The substrate 10 is [place] placed in the sputtering chamber in an atmosphere set to a temperature of 250°C. It is preferable that the substrate 10 be kept at 250°C for at least 3 minutes.

In the claims

Claim 1 has been amended as follows:

1. (Amended) A semiconductor device which comprises[;]:

a substrate, on a main surface of which, an interconnect [layers] layer made at

least of copper [are] is formed along with a predetermined pattern in buried condition in said substrate

an etching-stop layer formed on said main surface of said substrate; and

an insulation layer formed on said etching-stop layer,

said semiconductor device further comprises a single damascene structure via hole provided on a main [surfacer] surface of said insulation layer and penetrating through said insulation layer and said etching-stop layer so that a bottom of said via hole reaches at a surface of said interconnect layer, and [wherein] a barrier layer continuously covering said main surface of said insulation layer an inside wall surface of said via hole and the surface of said interconnect layer integratedly.